Amendments to the Specification:

Amendments directed to the specification herein with respect to paragraph numbers are made with respect to the application as filed.

Please replace the Abstract with the following amended paragraph:

ABSTRACT

Methods and devices for encoding in parallel a set of data bits for use in communications systems. The set of data bits to be encoded is divided into two subsets with the first subset being encoded in parallel using the second subset. The first subset is also encoded in parallel using the second subset. The first subset is also encoded in parallel using a subset of an immediately preceding set of data bits. Parallel encoding is realized by using an encoding module utilizing multiple single bit submodule. Each submodule receives a single bit from the first subset and either the second subset or the subset of the immediately preceding data set. Each single bit submodule produces a pair of output bits from the convolutional encoding of a single bit of the first subset and either the second subset [[of]] or the subset of the immediately preceding data set. The multiple single bit submodules operate in parallel to simultaneously and collectively produce a set of data bits.

Please replace paragraph [00009] with the following amended paragraph:

[00009] In a first aspect, the present invention provides a method for encoding a plurality of data bits for use in communications device, the method comprising:

a) receiving a set of data bits for encoding;

b) encoding in parallel a subset of said set of data bits using at least one other subset of data bits to produce at least one first set of output bits;

c) encoding in parallel said subset of said set of data bits using at least one previous subset of data bits to produce at least one second set of output bits, ~~the or each of~~ said previous subset being a subset of a previous set of data bits.

Please replace paragraph [00010] with the following amended paragraph:

[00010] In a second aspect, the present invention provides a method for encoding a set of data bits for use in a communications system, the method comprising the steps of:

a) receiving first and second subsets of said set of data bits;

b) convolutionally encoding said first subset using said second subset to produce a first set of output bits;

c) convolutionally encoding said first subset using a previous subset of an immediately preceding set of data bits to produce a second set of output bits; and

d) replacing said previous subset with said second subset of said set of data bits for use with a next set of data bits,

wherein said ~~encoding~~ encodings in steps b) and c) are executed in a bitwise parallel manner.

Please replace paragraph [00011] with the following amended paragraph:

[00011] In a third aspect, the present invention provides a device for encoding a set of data bits for use in a communications system, the device comprising:

first receiving means for receiving and storing a first subset of said set of data bits;

second receiving means for receiving and storing a second subset of said set of data bits;

storage means for storing a subset of an immediately preceding set of data bits;

first encoding means for convolutionally encoding a subset of data bits, said first encoding means receiving inputs from said first receiving means and from said second receiving means to produce a first set of output bits;

second encoding means for convolutionally encoding a subset of data bits, said second encoding means receiving inputs from said first receiving means and from said storage means to produce a second set of output bits;

switching means for storing contents of said second receiving means in said storage means,

wherein said storage means and said switching means [[is]] are activated after said first and second sets of output bits have [[bee]] been produced.

Please replace paragraph [00012] with the following amended paragraph:

[00012] In a fourth aspect, the present invention provides a system for encoding a current set of data bits for use in a communications device, the device comprising:

at least two encoding stages for encoding a subset of said current set of data bits, each of said at least two stages comprising:

first receiving means for receiving and storing a first subset of said current set of data bits;

storage means for storing a subset of data bits, said subset of data bits being chosen from a group comprising:

a second subset of said current set of data bits; and

a subset of a previously received set of data bits,

encoding means for encoding contents of said first receiving means using contents of said storage means to produce a set of output bits,

wherein at least one encoding stage receives a subset of data bits [[form]] from another encoding stage for storage in said storage means and for encoding a subset of said current set of data bits.

Please replace paragraph [00015] with the following amended paragraph:

[00015] In operation, the encoder system 5 receives in parallel a current set of data bits to be encoded by way of the bus 10. The current set of data bits (CURRENT [11:0]) is separated into two subsets with a [[fist]] first subset being fed into the first receiving means 20 and a second subset begin fed into the second receiving means 30. The storage means 40 stores a subset (PREVIOUS [11:6]) of an immediately preceding set of data bits. Once the current set of data bits are stored in the first and second receiving means, these are sent to the encoding modules 50, 60 with the first encoding module 50 receiving the first and second subsets of the current set of data bits. The second encoding module 60 receives the first subset and the subset stored in the storage means 40. The encoding modules 50, 60 then ~~encodes~~ encode, in a parallel bitwise manner, the first subset using the second subset and the subset stored in the storage means 40. Each encoding module independently produces a set of output bits which, when taken together, comprise the output of the encoder system 5. The encoder system output can then be fed into another bus (not shown) for transportation to a next stage in processing.

Please replace paragraph [00016] with the following amended paragraph:

[00016] It should be noted that, for this embodiment of the invention, convolutional encoding is performed by the encoding modules 50, 60. Furthermore, for this embodiment the bus 10 is a 12 bit bus carrying a current set of 12 bits with each subset having 6 data bits. The 6 LSB (least significant bits CURRENT [5:0]) of the 12 bit current set is fed and stored by the first receiving means 20 while the 6 MSB (most significant bits CURRENT [11:6]) of the 12 bit current set is fed and stored by the second receiving means 30. The storage means 40 receives the second subset (PREVIOUS [11:6]) stored in the second receiving means 30 when a new current set of data bits is clocked into the second receiving means. [[The]] A switching means for storing the contents of the second receiving means 30 can ~~be clocked into~~ also feed into the storage means 40. Alternatively, the switching/storing can be done as soon as the set of output data bits are produced. To initiate the encoder system, all zeros are set as the content of the storage means 40.

Please replace paragraph [00017] with the following amended paragraph:

[00017] It should further be noted that for convolutional encoding, and for the embodiment illustrated, each of the encoding modules produce a 12 bit output set. Furthermore, the storage means 40 and the first and second receiving means 20, 30 can be constructed as registers or suitable flip-flop circuits. Data subsets can then be clocked into [[he]] the registers or flip-flops in parallel and can also be fed in parallel into the encoding modules 50, 60.

Please replace paragraph [00019] with the following amended paragraph:

[00019] Each encoding module may be implemented as illustrated in FIG. 2. As can be seen in FIG. 2, a number of single-bit encoding submodules 70A-70F are present with each submodule receiving 7 data inputs--a single bit from the first subset (one of CURRENT [5:0]) and 6 bits from either the second subset (CURRENT 11:6]) or the subset stored in the storage means (PREVIOUS [11:6]). The single bit to be encoded is encoded using the other 6 bit input to result in two output bits. These output bits (x[0], y[0] to x[5], y[5]) comprise the output set of bits for the encoding module. Each submodule implements a combinational logic circuit that accomplishes the encoding. In one embodiment, the logic to be implemented for encoding IEEE 802.11a or Hiperlan 2 bitstreams is similar. The x and y equations for these two standards are as follows:

x[n]={XOR (in, s[4], s[3], s[1], s[0])}

y[n]={XOR (in, s[5], s[4], s[3], s[0])}

with in[[-]]=nth input bit from current set[[.]];

s[a]=the ath bit from the 6 bit input to the single bit encoding submodule.

Please replace paragraph [00021] with the following amended paragraph:

[00021] The above concepts and designs can therefore encode, in a parallel bitwise manner, a set of current data bits. To extend its capabilities, the system 5 in FIG. 5 can be seen as a two stage encoding system with each stage having three components--a first receiving means (such as receiving means 20), a storage means (such as receiving means 30 or storage means 40), and an encoding module which encodes the data in the first receiving means using the [[dat]] data in the storage means. Multiple stages can therefore be either cascaded or placed in parallel to encode multiple bit sets of data bits. Furthermore, the cascading need not be merely in terms of the output bits being cascaded in successive stages. The inputs may also be cascaded such as in the

embodiment explained above where a current input subset (such as CURRENT [11:6]) is subsequently used by a later stage in a succeeding step (such as becoming the subset PREVIOUS [11:6]).

Please replace paragraph [00022] with the following amended paragraph:

[00022] While the above embodiment convolutionally encodes a set of data bits, other encoding schemes may be used by changing or amending the internal combinational logic circuit used by the single-bit encoding submodule or by rearranging the sequence and/or position of the encoding stages as explained above. It should also be noted that other bit widths other than a 12 bit set or a 6 bit subset may be used. Furthermore, the design may be extended to other encoding schemes so that not all of the resulting or output bits of the encoder system 5 [[is]] may be valid or useful. For the convolutional system explained above, different coding rates produce different numbers of valid or useful bits. As an example, for a coding rate of 1/2, all 24 outputs bits from the encoder system 5 are valid. However, for a coding rate of 2/3 only the 18 LSB bits are valid. For this encoding rate, only 6 bits of the output set produced by the encoding module 50 are valid. For a coding rate of 3/4, only the 16 LSB bits of the overall set output are valid. Thus, only 4 bits of the output set produced by the encoding module 50 are valid.